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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/830,235	04/24/2001	Aaron Hal Dinwiddie	RCA-89210	4995

7590 06/13/2005

Joseph S Tripoli
Thomson Multimedia Licensing Inc
PO Box 5312
Princeton, NJ 08540

EXAMINER	
CASIANO, ANGEL L	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/830,235	DINWIDDIE ET AL.	
	Examiner	Art Unit	
	Angel L. Casiano	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-7 and 9-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-7 and 9-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. The present Office action is in response to Amendment submitted 11 March 2005.

2. Claims 1, 5-7, and 9-17 are pending in the application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5-7, and 9-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayes et al. [US 6,223,348 B1] in view of Charles et al. [US 6,044,215].

Regarding claim 1, Hayes et al. teaches an apparatus for loading computer code (see Abstract; col. 2, lines 27-30; col. 3, line 58). In addition, Hayes et al. discusses a memory card *preloaded* with computer code (see "code data", col. 6, lines 36-38). The apparatus, as disclosed, teaches a card interface (see col. 5, line 54) capable of distinguishing between card types (see col. 6, line 61). As it is well known in the art, integrated circuit cards and memory cards are types of storage devices in card format. The apparatus, as cited by Hayes et al. teaches memory for storing computer code for execution (see col. 6, lines 66-67). Hayes et al. explicitly teaches a computer controlled device memory unit (see col. 7, line 8) for storing a computer code that is downloaded (see col. 8, lines 10-12) from the memory unit of the memory card. The

Hayes et al. reference fails to teach a "card interface having a *first data port* and a *second data port*", "for transferring data in accordance with a first (second) *standard*". The cited reference also fails to teach a "*microcontroller* coupled to the card interface and to the memory for, if said card is a memory card, reading said computer code from said memory card by way of said second data port to said memory, for thereby updating the computer code stored in said memory so as to effect a change of the functional operation of the apparatus". Regarding these limitations, Charles et al. teaches an apparatus, providing interface having first and second data ports (see Figure 1A). In addition, Charles et al. teaches a controller (see col. 17, line 48). The Charles et al. reference teaches ports in accordance with different standards (see col. 17, lines 12-19). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a system for interfacing devices complying with different standards, allowing them to be used with portable computers, as taught by Charles et al (see col. 3, lines 28-34).

As for claim 5, Hayes et al. teaches means for producing a first signal coupled to an integrated circuit card connection and means for analyzing a second signal produced by a memory card in response to the first signal (see col. 12, lines 1-3; col. 6, lines 57-63).

As for claim 6, integrated circuit cards that are not memory cards do not produce the cited signal (see "correct type", col. 6, lines 57-63).

In consideration of claim 7, Hayes et al. teaches applying a signal to a clock signal connector of the integrated circuit card connection (see col. 7, line 45) as well as receiving a second signal on a data input/output signal connector of the integrated circuit card connection (see col. 7, lines 43-44).

As for claim 9, Hayes et al. teaches transferring computer code from the memory card to a computer controlled device memory unit (see col. 3, lines 55-61; col. 6, lines 65-67).

Considering claim 10, Hayes et al. teaches means for accepting or rejecting the computer code for transference from the memory card to a computer controlled device memory unit (see col. 6, lines 65-67; col. 7, lines 1-12).

Regarding claim 11, Hayes et al. teaches a method for loading computer code (see Abstract; col. 2, lines 27-30; col. 3, line 58) in a computer-controlled device. Hayes et al. also teaches a smart card interface for receiving a smart card (see col. 7, lines 33-39). The disclosed method teaches a card interface (see col. 5, line 54) capable of distinguishing (identifying) card types (see col. 6, line 61). As it is well known in the art, integrated circuit cards and memory cards are types of storage devices in card format. Hayes et al. discloses a computer controlled device memory (see col. 7, line 8) for storing a computer code that is transferred (see col. 8, lines 10-12) from the memory card. Nonetheless, Hayes et al. does not explicitly teach a memory card having a *first data port* for the step of transferring the computer code. The cited art does teach the application of a memory card for high-speed communication purposes (see col. 1, line 44;

col. 2, lines 36-38; col. 3, lines 51-52). Regarding these limitations, Charles et al. teaches an apparatus and method (see Abstract), providing interface having first and second data ports (see Figure 1A). In addition, Charles et al. teaches a controller (see col. 17, line 48). The Charles et al. reference teaches ports in accordance with different standards (see col. 17, lines 12-19). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a system for interfacing devices complying with different standards, allowing them to be used with portable computers, as taught by Charles et al (see col. 3, lines 28-34).

As for claim 12, Hayes et al. teaches a method including applying a first signal coupled to a memory card connection and analyzing a second signal produced by a memory card in response to the first signal (see col. 12, lines 1-3; col. 6, lines 57-63). In addition, Hayes et al. teaches a method capable of identifying card types (see col. 6, line 61).

As for claim 13, Hayes et al. does not teach a method including activating an NRSS interface. However, NRSS-type cards are well known in the art. In addition, Hayes et al. teaches an interface providing a clock signal. It would have been obvious to one of ordinary skill in the art at the time the invention was made that NRSS cards constituted a specific type of the memory cards, as disclosed by Hayes et al.

Considering claim 14, Hayes et al. teaches a method including the step of analyzing a header of the computer code to determine the validity of the computer code (see 6, line 64).

As for claim 15, Hayes et al. teaches toggling a reset signal (inherent, see col. 7, lines 41-47).

As for claim 16, Hayes et al. teaches monitoring a clock input signal terminal for a first signal in response to the toggled signal (inherent, see col. 7, lines 41-47).

As for claim 17, Hayes et al. teaches a method where a second signal is generated in response to detection of a first signal (see col. 7, lines 41-47).

Response to Arguments

5. Applicant's arguments with respect to claims 1, 5-7, and 9-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Kimura et al. [US 5522049 A] teaches a semiconductor disk device that is capable of processing hardware interface utilizing the basic input/output systems of various and different standard operating systems.
- Irisawa [JP 10069529 A] teaches an IC card.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 571-272-4142. The examiner can normally be reached on 9:00-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 571-272-4146. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alc
08 June 2005

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100